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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/008,272	11/13/2001	Benjamim Tang	35706.4500	2550

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EXAMINER	
BURD, KEVIN MICHAEL	
ART UNIT	PAPER NUMBER
2631	4

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DATE MAILED: 02/17/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/008,272	TANG, BENJAMIM	
	Examiner	Art Unit	
	Kevin M Burd	2631	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 October 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 November 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 2-3.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

1. Claims 1, 2 and 4-16 are rejected under 35 U.S.C. 102(e) as being anticipated by Carlson (US 6,167,526).

Regarding claims 1, 2 and 8, Carlson discloses a system for synchronizing an output signal to a data signal in figure 3. A data signal is received in elements 324 and 326. The data signal is compared to a window signal that is adjusted by the output signal (figure 3 and column 4, lines 25-46) to determine if the data signal is an early or late pulse. Since it is determined if the pulse is early or late, the data transitions of the pulse are determined to be either early or late. A timing signal is generated by these elements indicating the phase relationship between the data signal and the window signal. These signals are output to the OR gates 352 and 353. The early signals are ORed together and form a "scaled down" timing signal. The late signals are ORed together and form a "scaled down" timing signal. These "scaled down" timing signals are input to the detection counter which outputs a adjust signal for adjusting the window signal (figure 3 and column 5, lines 7-28). The detection counter is an "integrator" in that

it outputs the signal that modifies the window signal. The detection counter will generate an early and late count from the outputs of the OR gates and will increment the count or decrement the count accordingly.

Regarding claims 4-7, the counts are incremented when an early or late pulse is detected. Any component of the pulse that is detected will indicate an early or a late pulse (column 7, lines 12-15).

Regarding claim 9, Carlson discloses a method for synchronizing an output signal to a data signal. Carlson discloses the circuit for conducting this method in figure 3. A data signal is received in elements 324 and 326. The data signal is compared to a window signal that is adjusted by the output signal (figure 3 and column 4, lines 25-46). A timing signal is generated by these elements indicating the phase relationship between the data signal and the window signal. These signals are output to the OR gates 352 and 353. The signals are ORed together and form "scaled down" timing signals. These "scaled down" timing signals are input to the detection counter which outputs a adjust signal for adjusting the window signal (figure 3 and column 5, lines 7-28). The detection counter is an "integrator" in that it outputs the signal that modifies the window signal.

Regarding claim 10, the window signals are used to determine if the data signal is an early or late data signal and allows for the generation of an early or late pulse in elements 324 and 326 (figure 3).

Regarding claim 11, as stated above, the signals are ORed together and form "scaled down" timing signals. These "scaled down" timing signals are input to the

detection counter which outputs a adjust signal for adjusting the window signal (figure 3 and column 5, lines 7-28). The detection counter is an "integrator" in that it outputs the signal that modifies the window signal.

Regarding claims 12 and 16, Carlson discloses a system for synchronizing an output signal to a data signal in figure 3. A data signal is received in elements 324 and 326 and these elements act as phase detectors. The data signal is compared to a window signal that is adjusted by the output signal (figure 3 and column 4, lines 25-46) to determine if the data signal is an early or late pulse. Since it is determined if the pulse is early or late, the data transitions of the pulse are determined to be either early or late. A timing signal is generated by these elements indicating the phase relationship between the data signal and the window signal. These signals are output to the OR gates 352 and 353. The early signals are ORed together and form a "scaled down" timing signal. The late signals are ORed together and form a "scaled down" timing signal. These "scaled down" timing signals are input to the detection counter which outputs a adjust signal for adjusting the window signal (figure 3 and column 5, lines 7-28). The detection counter is an "integrator" in that it outputs the signal that modifies the window signal.

Regarding claims 13-15, the detection counter 370 outputs an adjustment signal that adjusts the window signal. The window signal determines if the data signal is an early or late signal (column 6, lines 42-59).

Allowable Subject Matter

2. Claim 3 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks
Washington, D.C. 20231

or faxed to:

(703) 872-9314, (for formal communications intended for entry or for informal or draft communications, please label "PROPOSED" or "DRAFT")

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth Floor (Receptionist).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kevin Burd, whose telephone number is (703) 308-7034. The Examiner can normally be reached on Monday-Thursday from 9:00 AM - 6:00 PM.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 305-3800.

Kevin M. Burd
PATENT EXAMINER
2/10/2004